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ART UNIT	PAPER NUMBER
2123	12

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Please find below and/or attached an Office communication concerning this application or proceeding.

PRE

Office Action Summary	Application No.	Applicant(s)	
	09/344,847	PANESAR, GAJINDER SINGH	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *05 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 August 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *9* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Introduction

1. This communication is in response to the Applicant's Response mailed on December 5, 2002. Claims 5 and 9 were amended. Claims 1-9 of the application are pending.

Response to Arguments

2. Applicant's arguments filed on December 5, 2002 have been fully considered. Claim rejection under 35 U.S.C. §101 is withdrawn in response to claim amendment. Applicants' arguments, filed on December 5, 2002 under 35 U.S.C. §103 (a) are persuasive. The art rejections are based on the additional prior art included in this office action. Therefore, this office action is made non-final.

Information Disclosure Statement

3. Acknowledgment is made of the information disclosure statements filed on February 27, 2003 together with copies of the patents and papers. The patents and papers have been considered in reviewing the claims.

Drawings

4. The drawings sent on August 10, 1999 are accepted by the examiner with the following objection:

In Fig. 7, "STATE PERIPUCAL" is incorrect. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

6. Claims 1-5, and 8-9 are rejected under 35 U.S.C. § 102(e) as being anticipated by **Aleksic et al. (AL)** (U.S. Patent 5,995,736).

6.1 **AL** teaches method and system for automatically modeling registers for integrated circuit design. Specifically, as per Claim 1, **AL** teaches a method of operating a computer system to design an application specific processor (ASP) (Col 1, Lines 6-9; Col 7, Lines 3-17; Fig. 4) comprising:

defining a set of peripherals for the ASP which are responsive to stimuli and which communicate with a processor (Col 1, Lines 13-16 and Lines 30-33; Col 1, Lines 36-38);

generating for each peripheral an input file which defines the functional attributes of that peripheral in a high level language with an input data structure (Col 1, Lines 13-16 and Lines 30-38; Fig 6A; Col 3, Lines 59-63; Col 9, Lines 7-19);

entering the input file into the computer system and operating a modelling tool loaded on the computer system to generate from the input file a register definition file by allocating specific elements of the input data structure to predefined sectors of a register definition table (Col 1, Lines 58 to Col 2, Line 18; Col 2, Lines 29-39 and Col 3, Line 53 to Col 4, Line 10; Fig 6A; Col 5, Lines 18-22); and

using the register definition file to create in silicon the registers of the ASP (Col 5, Lines 19-29; Fig. 1, Block 30; Fig. 3, Block 62; Fig. 4, Block 38; Col 4, Lines 55-57).

6.2 As per Claim 2, **AL** teaches the method of Claim 1. **AL** also teaches that each input file comprises a data structure which defines for each of a set of registers the name of an element in the register, the bit length of the element, the functional status of the element and the function of the element (Col 3, Lines 60-66 and Figure 7, Blocks 49, 132 and 134; Col 12, Lines 1-30).

6.3 As per Claim 3, **AL** teaches the method of Claim 1. **AL** also teaches that each register definition table includes at least predefined sectors for the bit location within a register of an element, the name of the element, the function of the element and the functional status of the element (Col 3, Lines 60-66 and Figure 7, Blocks 49, 132 and 134; Col 12, Lines 1-30).

6.4 As per Claim 4, **AL** teaches the method of Claim 1. **AL** also teaches that the register definition table includes the word location of the register within a memory map for access during simulation of the ASP (Col 3, Lines 63-66; Col 11, Lines 60-67).

6.5 As per Claim 5, **AL** teaches a computer system which comprises a processor and a memory, the memory holding a program representing a modelling tool for use in designing an application specific processor (ASP) (Col 1, Lines 6-9; Col 3, Line 53 to Col 4, Line 10; Fig. 4; Col 7, Lines 3-17);

the computer system comprises an input means for receiving a plurality of input files, each input file defining the functional attributes of a peripheral for the ASP in a high level language within an input data structure (Col 1, Lines 13-16 and Lines 30-38; Fig 6A; Col 3, Lines 59-63; Col 9, Lines 7-19);

the processor being operable to execute the program representing the modelling tool to generate from the input file a register definition file by allocating specific elements of the input data structure to predefined sectors of a register definition table (Col 1, Lines 58 to Col 2, Line 18; Col 2, Lines 29-39 and Col 3, Line 53 to Col 4, Line 10; Fig 6A; Col 5, Lines 18-22); and

the computer system comprises an output means for outputting the register definition file in a manner which is usable to create in silicon the registers of the ASP (Col 5, Lines 19-29; Fig. 1, Block 30; Fig. 3, Block 62; Fig. 4, Block 38; Col 4, Lines 55-57).

6.6 As per Claim 8, **AL** teaches a computer program product stored on a computer readable medium and comprising software code portions operable when executed by a computer to read an input file which defines an input date structure the functional attributes of a peripheral for an application specific processor in a high level language (Col 1, Lines 6-9; Fig. 4, Block 79; Col 1, Lines 13-16 and Lines 30-38; Col 3, Line 53 to Col 4, Line 3; Fig 6A; Col 9, Lines 7-19); and

to generate from that input file a register definition file, the software code portions including a code portion for allocating specific elements of the input data structure to predefined sectors of a register definition table for each of a plurality of registers (Col 1, Lines 58 to Col 2, Line 18; Col 2, Lines 29-39 and Col 3, Line 53 to Col 4, Line 10; Fig 6A; Col 5, Lines 18-22).

6.7 As per Claim 9, **AL** teaches a register definition file stored on a computer readable medium and comprising a plurality of register definition tables (Col 3, Lines 66 to Col 4, Line 7; Col 5, Lines 19-30);

each table including at least predefined sectors for the bit location within a register of an element, the name of the element, the function of the element and the functional status of the element (Fig. 7, Item 49, 132 and 134; Col 12, Lines 1-30); and

each table including the word location of the register within a memory map wherein the computer readable medium is loaded into a computer for simulating an application specific processor, the register definition tables are accessed based on the word location for simulation of the registers (Fig. 2, Block 38; Col 5, Lines 22-24; Col 6, Lines 18-22; Col 7, Lines 3-17 and Col 11, Lines 60-67).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Aleksic et al. (AL)** (U.S. Patent 5,995,736) in view of **Sharma et al. (SH)** (U.S. Patent 5,491,640).

9.1 As per Claim 6, **AL** teaches the computer system of Claim 5. **AL** teaches a hardware system for implementing the system for automatically modeling registers for the IC design, which includes memory and processor for storing and processing requisite template and file information to automatically generate behavior model register code and hardware design simulation code. The hardware may be any suitable computer and preferably is a workstation based computer system (Fig. 3, Block 34; Col 7, Lines 3-10).

AL does not expressly teach that the input means comprises means for receiving a physical recording device holding the input file for each peripheral. **SH** teaches that the input means comprises means for receiving a physical recording device holding the input file for each peripheral (Fig 2a, Block 42; Col 4, Lines 40-56), as the physical recording device holding the input file for each peripheral such as the removable storage device allows transfer of data to and from the computer system (Col 4, Lines 55-56). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer system of **AL** with the computer system of **SH** that included the input means comprising means for receiving a physical recording device holding the input file for each peripheral, as the physical recording device holding the input file for each peripheral such as the removable storage device would allow transfer of data to and from the computer system.

9.2 As per Claim 7, **AL** teaches the computer system of Claim 5. **AL** teaches a hardware system for implementing the system for automatically modeling registers for the IC design, which includes memory and processor for storing and processing requisite template and file information to automatically generate behavior model register code and hardware design simulation code. The hardware may be any suitable computer and preferably is a workstation based computer system (Fig. 3, Block 34; Col 7, Lines 3-10). **AL** also teaches that design changes occur throughout the design process, so the register layer may change with the design change; when a previous register layer exists, the automatic register generator determines the differences in the previous layer and the merged layer (Col 6, Lines 38-46). So it is obvious that

the register layer is saved as templates and files in the computer's external memory in between design changes, the external memory being a disk or a tape.

AL does not expressly teach that the output means comprises means for loading the register definition file onto a physical recording device. **SH** teaches that the output means comprises means for loading the files onto a physical recording device, such as mass storage or removable storage (Fig 2a, Block 42; Col 4, Lines 40-56), as the physical recording device holding register definition file such as the removable storage device allows transfer of data to and from the computer system (Col 4, Lines 55-56). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the computer system of **AL** storing register definition file onto an external memory with the computer system of **SH** that included the output means comprising means for loading the files onto a physical recording device, as the physical recording device holding register definition file such as the removable storage device would allow transfer of data to and from the computer system.

Applicant's Arguments

10. The applicant argues the following:

(1) with regard to Claim 1, the Office Action failed to establish a prima facie case of obviousness; there is no suggestion in the references that would motivate one of ordinary skill in the art to combine the references;

(2) the inputs disclosed by SH are provided in a low-level hardware description language such as HDL;

(3) neither AL nor SH disclose allocating elements from the input data structure to predefined register definition table;

(4) neither AL nor SH disclose receiving a physical recording device holding the input file for each peripheral; and

(5) neither AL nor SH disclose loading a register definition file onto a physical recording device.

Examiner's reply

11. As per the applicant's arguments, the applicant's attention is requested to the corresponding claim rejections. In addition, the following explanation is provided to further explain the examiner's position.

11.1 As per the applicant's argument that "with regard to Claim 1, the Office Action failed to establish a prima facie case of obviousness; there is no suggestion in the references that would motivate one of ordinary skill in the art to combine the references", the examiner has identified relevant references in the primary reference itself, thus not requiring to use the secondary reference.

11.2 As per the applicant's argument that "the inputs disclosed by SH are provided in a low-level hardware description language such as HDL", the examiner has identified the reference in the primary reference where the input file is in a higher level language. AL teaches generating for each peripheral an input file which defines the functional attributes of that peripheral in a

high level language with an input data structure (Col 1, Lines 13-16 and Lines 30-38; Fig 6A; Col 3, Lines 59-63; Col 9, Lines 7-19).

11.3 As per the applicant's argument that "neither AL nor SH disclose allocating elements from the input data structure to predefined register definition table", the examiner has identified the reference in the primary reference where elements from the input data structure are allocated to predefined register definition table. AL teaches generating from the input file a register definition file by allocating specific elements of the input data structure to predefined sectors of a register definition table (Col 1, Lines 58 to Col 2, Line 18; Col 2, Lines 29-39 and Col 3, Line 53 to Col 4, Line 10; Fig 6A; Col 5, Lines 18-22)

11.4 As per the applicant's argument that "neither AL nor SH disclose receiving a physical recording device holding the input file for each peripheral", the examiner has used a new reference (**SH**).

11.5 As per the applicant's argument that "neither AL nor SH disclose loading a register definition file onto a physical recording device", the examiner has used a new reference (**SH**).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure.

The following patents are cited to further show the state of the art with respect to automatically modeling registers for an Integrated circuit.

1. Sharma et al., "Method and apparatus for synthesizing datapaths for integrated circuit design and fabrication", U.S. Patent 5,491,640, February 1996.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-746-7329.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
May 7, 2003

SAMUEL BRODA, ESQ.
PRIMARY EXAMINER